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| First Named Inventor  | Leonard Forbes    | <b>INFORMATION DISCLOSURE<br/>STATEMENT<br/>FORM PTO-1449</b> |
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| Examiner Name   | Unknown           |   |
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| Attorney Docket No.   | 400.272US01       |   |
| Title: NROM FLASH MEMORY WITH HIGH-PERMITTIVITY GATE DIELECTRIC |                   | Sheet 1 of 7  |

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| Title: NROM FLASH MEMORY WITH HIGH-PERMITTIVITY GATE DIELECTRIC |                   | Sheet 2 of 7  |

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| Title: NROM FLASH MEMORY WITH HIGH-PERMITTIVITY GATE DIELECTRIC |                   | Sheet 7 of 7  |

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| TH | J. Bu, et al., "Retention Reliability Enhanced SONOS NVSM with Scaled Programming Voltage," Microelectronics Lab., Date Unknown   |
| TH | H. Tomiye, et al., "A novel 2-bit/cell MONOS memory device with a wrapped-control-gate structure that applies source-side hot-electron injection," 2002 Symposium on VLSI Technology Digest of Technical Papers, Copyright 2002 IEEE. |
| TH | Certified Translation, "Flash cell that seeks to replace current technology introduced enabling both low cost and high performance" Nikkei Microdevices, November 1999, pp. 147-148.  |

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|---|-----------|-----------------|-----------|
| Examiner Signature  | TH TH +10 | Date Considered | Feb. 2005 |
| <small>*Examiner: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.</small> |           |                 |           |